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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WANG, ALBERT C	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 10/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/800,851	HUTTON ET AL.
	Examiner	Art Unit
	Albert Wang	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed 15 July 2004, in which new claims 21-29 are added.

Specification

2. The disclosure is objected to because of the following informalities: "[s]peed banning" in paragraph 3 is interpreted as "speed binning".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 27 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. While LTRAN oscillator 130 and RTRAN oscillator 135 are shown in figure 1 and mentioned paragraphs 11 and 12, no where in the specification are the terms LTRAN and RTRAN associated with a process parameter..

4. Claims 23 and 25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites the limitation "a third circuit". There is insufficient antecedent basis for this limitation in the claim since there is no "second circuit".

The phrase "physically close to each other" in claim 25 is a relative term which renders the claim indefinite. The phrase "physically close to each other" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 10, 21-26, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Stinson et al., U.S. Patent No. 6,553,545 ("Stinson").

As per claim 1, Stinson discloses a method for detecting process variations, the method comprising:

controlling count gate control by a first circuit (fig. 1, by mux 17; col. 2, lines 40-50; col. 3, lines 5-14);

generating at least one clock count by a second circuit (fig. 1, by counter 16; col. 3, lines 5-14); and

outputting results of the clock count by a third circuit (fig. 1, by shift register 12; col. 3, lines 25-34).

As per claim 10, Stinson discloses an apparatus to detect process variations comprising:

a first circuit to select a clock (fig. 1, mux 17; col. 2, lines 40-50; col. 3, lines 5-14);

a second circuit connected to the first circuit to generate at least one clock count (fig. 1, counter 16; col. 3, lines 5-14); and

a third circuit connected to the first circuit to output a result of the clock count (fig. 1, shift register 12; col. 3, lines 25-34).

As per claim 21, Stinson discloses a method for detecting variations, comprising:

controlling count gate control by a first circuit to select a first oscillator(fig. 1, by mux 17 to select a first test structure from a plurality of test structures; col. 2, lines 40-50; col. 3, lines 5-14);

generating a clock by the first oscillator in a second circuit (fig. 1, col. 2, lines 40-50, by the first test structure in circuit 18);

counting the clock generated by the first oscillator by a third circuit (fig. 1, by counter 16; col. 3, lines 5-14);

outputting a count of the clock generated by the first oscillator by the third circuit (fig. 1, by shift register 12; col. 3, lines 25-34);

selecting a second oscillator in the second circuit (col. 3, lines 5-14, selection based on command);

generating a clock by the second oscillator in the second circuit (col. 3, lines 5-14);

counting the clock generated by the second oscillator by the third circuit (col. 3, lines 5-14); and

outputting a count of the clock generated by the second oscillator by the third circuit (col. 3, lines 25-34).

As per claim 22, Stinson discloses a third oscillator for which corresponding steps may be taken (figs. 10 & 11).

As per claim 23, Stinson discloses an apparatus to detect process variations comprising:

a first circuit to control count gate control (fig. 1, mux 17; col. 2, lines 40-50; col. 3, lines 5-14);

a first oscillator to generate a clock (fig. 1, col. 2, lines 40-50, a first test structure of a plurality in circuit 18), wherein the first circuit is to select the clock generated by the first oscillator (col. 3, lines 5-14);

a third circuit to count the clock generated by the first oscillator and to output the count of the clock generated by the first oscillator (col. 3, lines 5-14 & 25-34, shift register 12); and

a second oscillator to generate a clock (col. 2, lines 40-50, a second test structure), wherein the first circuit is to select the clock generated by the second oscillator (col. 3, lines 5-14), and the third circuit is to count the clock generated by the third oscillator and is to output the count of the clock generated by the third oscillator (col. 3, lines 5-14 & 25-34).

As per claim 24, Stinson discloses a third oscillator for which corresponding steps may be taken (figs. 10 & 11).

As per claim 25, Stinson discloses the oscillators are physically closes to each other (figs. 10 & 11).

As per claim 26, Stinson discloses a standard ring oscillator (fig. 3; col. 3, lines 53-55).

As per claim 29, Stinson discloses a multiplexer (fig. 1, mux 17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-9 and 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stinson as applied to claim 1 above, and further in view of IEEE Std 1149.1-1990, "IEEE Standard Test Access Port and Boundary-Scan Architecture", (includes IEEE Std 1149.1a-1993), 1993 ("IEEE").

As per claim 8, while Stinson teaches communicating with a test access port interface (col. 3, lines 25-34), Stinson is silent with respect to a JTAG interface. IEEE teaches an interface standard that is commonly referred to as JTAG (page iii). At the time of the invention, it would have been obvious to one skilled in the art to apply IEEE's standard to Stinson's test access port, since IEEE's standard is a well-known standard for test access ports.

As per claim 2, IEEE teaches the controlling comprises: activating a scan signal (sec. 3.4, TDI); toggling a clock signal (sec. 3.2, TCLK); and setting a reset signal on (sec. 5.3, TRST).

As per claim 3, IEEE teaches controlling further comprises the steps of: selecting an oscillator by activating and toggling the signals; enabling the oscillator ; and setting the reset signal off (sec. 5.3, 8.1 & 10.2).

As per claim 4, Stinson teaches the controlling further comprises the step of toggling the clock signal for a period of time (col. 3, lines 5-14).

As per claim 5, Stinson teaches the step of generating further comprises the steps of: outputting the count into a counter (fig. 1, into counter 16); and reading the count into a scan chain (fig. 1, into shift register 12).

As per claim 6, Stinson teaches toggling further comprises the step of storing the output of the toggle in a counter (col. 3, lines 15-21).

As per claim 7, IEEE teaches the step of toggling a clock for reading out the clock count (sec. 8.1 & 10.2).

As per claim 9, IEEE teaches communicating with a JTAG interface (page iii).

As per claim 11, IEEE teaches the first circuit comprises: a scan signal; and a clock signal, wherein the scan signal and the clock signal turn on at least one clock (sec. 3.2, 3.4 & 8.1).

As per claim 12, IEEE teaches the first circuit further comprises: a reset signal; and an enable signal, wherein the enable signal enables the at least one clock (sec. 5.3 & 8.1).

As per claim 13, Stinson teaches the clock signal is toggled for a period of time (col. 3, lines 5-14).

As per claim 14, Stinson teaches the second circuit further comprises outputting a count of the toggle (col. 3, lines 15-21).

As per claim 15, Stinson teaches the third circuit comprises: a counter; and a scan chain, wherein the scan chain is connected to the counter (col. 3, lines 15-34).

As per claim 16, Stinson teaches the at least one count is input to the counter (col. 3, lines 15-34).

As per claim 17, IEEE teaches the reset signal is input to the counter (sec. 5.3).

As per claim 18, IEEE teaches the scan chain further comprises a read signal, wherein the read signal reads the count into the scan chain (sec. 8.1 & 10.2).

As per claim 19, IEEE teaches the clock signal is toggled to read out the count from the scan chain (sec. 8.1 & 10.2).

As per claim 20, IEEE teaches the scan chain communicates with a JTAG interface (page iii).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100